WHAT IS CLAIMED IS:

1. A logic circuit, comprising:

a first inversion section for inverting a first input signal having one of positive logic and negative logic and outputting the inverted signal;

a second inversion section for inverting a second input signal having the other of the positive logic and the negative logic and outputting the inverted signal; and

a transmission section for selectively outputting one of the output of said first inversion section and the output of said second inversion section in accordance with a logical value which depends upon an externally controllable selection signal and an inverted signal of the selection signal.

2. A logic circuit, comprising:

a first inversion section for inverting a first input signal and outputting the inverted signal;

a second inversion section for inverting a second input signal and outputting the inverted signal;

a first outputting section for selectively outputting one of the output of said first inversion section and the output of said second inversion section in accordance with a logical value which depends upon an externally controllable first selection signal and an inverted signal of the first selection signal; and

a second outputting section for selectively

outputting one of the output of said first inversion section and the output of said second inversion section in accordance with a logical value which depends upon an externally controllable second selection signal and an inverted signal of the second selection signal.

3. A logic circuit, comprising:

a first inversion section for inverting a first input signal and outputting the inverted signal;

a second inversion section for inverting a second input signal and outputting the inverted signal; and

a transmission section capable of discriminating a magnitude relationship of 1 bit between the first input signal and the second input signal and outputting a result of the discrimination using a plurality of status signals.

4. The logic circuit according to claim 3, wherein said transmission section includes a first gate section for indicating whether or not the first input signal is equal to or greater than the second input signal, a second gate section for indicating whether or not the first input signal is greater than the second input signal, a third gate section for indicating whether or not the first input signal is equal to or smaller than the second input signal, and a fourth gate section for indicating whether or not the first input signal is smaller than the second input signal.

5. A logic circuit, comprising:

a first comparison section for receiving a first input signal of n_1 bits and a second input signal of n_1 bits, performing magnitude comparison between a predetermined number of bits of the first input signal and the predetermined number of bits of the second input signal and outputting results of the comparison of the predetermined number of bits as a p_1th comparison result, a p_2th comparison result, a p_3th comparison result and a p_4th comparison result using a plurality of status signals, n_1 being an integer equal to 2 to the m_1th power, m_1 being an even number equal to or greater than 2;

a second comparison section for performing magnitude comparison between a number of bits equal to twice the predetermined number of bits of the first input signal and a number of bits equal to twice the predetermined number of bits of the second input signal from the p_1th comparison result and the p_2th comparison result and outputting a result of the comparison of the predetermined number of bits as a p_5th comparison result using the plurality of status signals and for performing magnitude comparison between a number of bits equal to twice the predetermined number of bits of the first input signal and a number of bits equal to twice the predetermined number of bits of the second input signal from the p_3th comparison result and the p_4th comparison result and outputting a result of the comparison of the predetermined number of bits as a p_6th comparison result

using the plurality of status signals; and

a third comparison section for performing magnitude comparison between the n_1 bits of the first input signal and the n_1 bits of the second input signal from the p_5th comparison result and the p_6th comparison result and outputting a result of the comparison of the n_1 bits using the plurality of status signals.

6. A logic circuit, comprising:

a half addition arithmetic section for receiving a first input signal of n_2 bits and an inverted signal of a second input signal of n_2 bits and performing half addition arithmetic of the first input signal and the inverted signal of the second input signal, n_2 being an integer equal to 2 to the m_2th power, m_2 being an even number equal to or greater than 2;

a first arithmetic section for performing full addition arithmetic of the first input signal and the inverted signal of the second input signal separately for each predetermined number of bits and outputting a result of the full addition arithmetic as a q_1th carry, a q_2th carry, a q_3th carry and a q_4th carry using a plurality of status signals;

a second arithmetic section for outputting logical AND information of the q_1th carry and the q_2th carry as a q_5th carry using the plurality of status signals and outputting logical AND information of the q_3th carry and the q_4th carry as a q_6th carry using the plurality of status

signals;

a third arithmetic section for outputting logical AND information of the carries of all of the n_2 bits as a q_7th carry using the plurality of status signals from at least the q_5th carry and the q_6th carry; and

a fourth arithmetic section for performing logical exclusive ORing of the output of said half addition arithmetic section and the q_7th carry and outputting a full addition arithmetic result.

7. A logic circuit, comprising:

a first inversion section for inverting a first input signal and outputting the inverted signal;

a second inversion section for inverting the inverted signal of the first input signal and outputting a resulting signal;

a first outputting section for performing NANDing arithmetic between the output of said first inversion section and a second input signal and outputting a resulting signal; and

a second outputting section for performing NANDing arithmetic between the output of said second inversion section and an inverted signal of the second input signal and outputting a resulting signal;

said first outputting section and said second outputting section being switched with the second input signal and the inverted signal of the second input signal.

8. The logic circuit as claimed in claim 1, further comprising:

a first switching section provided on an input side of said first inversion section and capable of performing switching of whether the first input signal should be passed or blocked in accordance with an external control signal; and

a second switching section provided on an input side of said second inversion section and capable of performing switching of whether the second input signal should be passed or blocked in accordance with the external control signal.

9. A logic circuit, comprising:

a first carry generation section for receiving a first input signal A<0: n_3> of n_3 bits and an inverted signal XA<0:n_3> of the first input signal of n_3 bits and outputting a first logical AND result and a first logical AND inversion result as a logical AND result at least of bits A<0> to A<2 to the m_3th power - 1> from the first input signal bits A<0: 2 to the m_3th power - 1> and the inverted signal bits XA<0: 2 to the m_3th power - 1>, n_3 being an integer equal to 2 to the m_3th power, m_3 being an even number equal to or greater than 2;

a second carry generation section for outputting a second logical AND result and a second logical AND inversion result as a logical AND result at least of bits

A<2 to the m_3th power> to A<2 × 2 to the m_3th power - 1> from the first input signal bits A<2 to the m_3th power: 2 × 2 to the m_3th power - 1> and the inverted signal bits XA<2 to the m_3th power: 2 × 2 to the m_3th power - 1>;

a third carry generation section for outputting a third logical AND result and a third logical AND inversion result as a logical AND result at least of bits A<2 × 2 to the m_3th power> to A<3 × 2 to the m_3th power - 1> from the first input signal bits A<2 × 2 to the m_3th power: 3 × 2 to the m_3th power - 1> and the inverted signal bits XA<2 × 2 to the m_3th power: 3 × 2 to the m_3th power - 1>;

a fourth carry generation section for outputting a fourth logical AND result and a fourth logical AND inversion result as a logical AND result at least of bits A<3 × 2 to the m_3th power> to A<4 × 2 to the m_3th power - 1> from the first input signal bits A<3 × 2 to the m_3th power: 4 × 2 to the m_3th power - 1> and the inverted signal bits XA<3 × 2 to the m_3th power: 4 × 2 to the m_3th power - 1>;

a first logical AND generation section for receiving the first logical AND result and the first logical AND inversion result as well as the second logical AND result and the second logical AND inversion result and outputting a fifth logical AND result and a fifth logical AND inversion result as a logical AND result at least of the bits A<0> to A<2 × 2 to the m_3th power - 1>;

a second logical AND generation section for

receiving the third logical AND result and the third logical AND inversion result as well as the fourth logical AND result and the fourth logical AND inversion result and outputting a sixth logical AND result and a sixth logical AND inversion result as a logical AND result at least of the bits A<2 × 2 to the m_3th power> to A<4 × 2 to the m_3th power - 1>;

a third logical AND generation section for outputting a seventh logical AND result and a seventh logical AND inversion section as a logical AND result at least of the bits A<0> to A<2 × 2 to the m_3th power - 1> from the fifth logical AND result and the fifth logical AND inversion result as well as the sixth logical AND result and the sixth logical AND inversion result;

a fourth logical AND generation section for outputting an eighth logical AND result and an eighth logical AND inversion result as a logical AND result at least of the bits A<2 to the m_3th power> to A<3 × 2 to the m_3th power - 1> from the second logical AND result and the second logical AND inversion result as well as the sixth logical AND result and the sixth logical AND inversion result; and

a full addition arithmetic section for outputting a full addition arithmetic result of n_3 bits from a first gate signal of n_3 bits which includes the seventh logical AND result, the eighth logical AND result, the sixth logical AND result and the fourth logical AND result and

a second gate signal of n_3 bits which includes the seventh logical AND inversion result, the eighth logical AND inversion result, the sixth logical AND inversion result and the fourth logical AND result.

10. The logic circuit as claimed in claim 3, wherein the plurality of status signals includes a first gate signal for indicating whether or not the first input signal is equal to or greater than the second input signal, a second gate signal for indicating whether or not the first input signal is greater than the second input signal, a third gate signal for indicating whether or not the first input signal is equal to or smaller than the second input signal, and a fourth gate signal for indicating whether or not the first input signal is smaller than the second input signal.

11. The logic circuit as claimed in claim 5, wherein the plurality of status signals includes a first gate signal for indicating whether or not the first input signal is equal to or greater than the second input signal, a second gate signal for indicating whether or not the first input signal is greater than the second input signal, a third gate signal for indicating whether or not the first input signal is equal to or smaller than the second input signal, and a fourth gate signal for indicating whether or not the first input signal is smaller than the second

input signal.

12. The logic circuit as claimed in claim 6, wherein the plurality of status signals includes a first gate signal for indicating whether or not the first input signal is equal to or greater than the second input signal, a second gate signal for indicating whether or not the first input signal is greater than the second input signal, a third gate signal for indicating whether or not the first input signal is equal to or smaller than the second input signal, and a fourth gate signal for indicating whether or not the first input signal is smaller than the second input signal.

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